IMX Pregius IP Core

IP CORE FOR SONY PREGIUS SUB-LVDS IMAGE SENSORS

AT A GLANCE

- SubLVDS readout and decoding block
- SPI-based sensor configuration module
- Software library for sensor configuration
- Free running or triggered readout modes

With the IMX Pregius, Sony offers a series of widely used, high quality CMOS imagers. S2I supports these sensors with a dedicated IP Core able to read sensor data and control the sensors. The IMX IP Core is delivered as a reference design along with an FMC module compatible with S2I MVDK and standard FPGA evaluation kits. Together, they provide an easy way to design a camera.

The IMX IP Core is made of the following blocks:

The **SubLVDS Receiver and Deserializer** block is connected to the imager's output pins and uses the FPGA IO cells to deserialize the image stream. This block is highly FPGA dependent and currently limited to Xilinx FPGAs. The parallel video stream can be optionally cropped and is presented in a Camera Link-like format for further processing.

The IMX sensor itself can be used in free running mode or in slave mode using the core's **timing and trigger generator.**

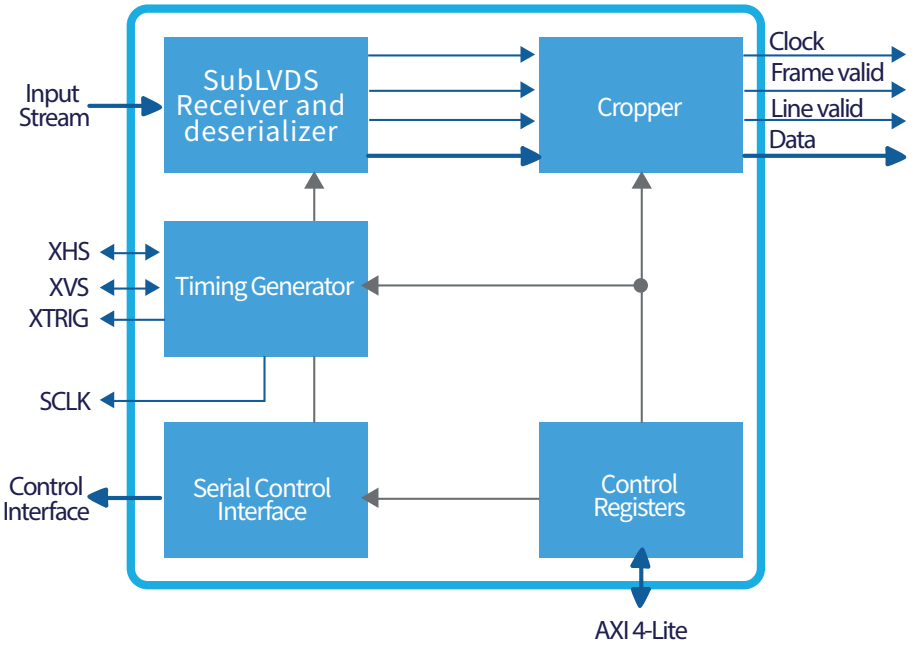
An SPI-based control interface enables sensor configuration, following the correct configuration timing.

The functionality of the IP core is configured either by parameters at compile time, or by **Control Registers** using an AXI-Lite interface at run time.

A C software library configures the sensor and the IP core.

Delivery

The IP core is delivered with a full reference design, including an FMC (FPGA Mezzanine Card), which forms the interface between the sensor and a standard FPGA evaluation board. The FMC module is FMC-LPC compliant and does all power and level adaptations required by the IMX CMOS sensor.



The following evaluation boards are compatible with the FMC module:

- S2I MVDK with ZX5 and ZX1 Zynq modules
- Xilinx Artix-7 FPGA AC701 Evaluation Kit
- Xilinx Kintex-7 FPGA KC705 Evaluation Kit

All these boards have a 1-Gbit Ethernet interface, so the reference design comes as a GigE Vision camera.

IMX Interface Board

AVAILABLE MODULES

MODULE	DESCRIPTION	ARTIX7	KINTEX7	ZYNQ7
IMX IP Core	SubLVDS IMX Pregius IP			
Encrypted VHDL		•	•	•
VHDL source		o	o	o
IMX IP Software library	API to control core and imager			
Object File		•	•	•
C-Source		o	o	o
Reference design with GigE Vision interface		•	•	•

RESOURCE USAGE

MODULE	ARTIX7	KINTEX7	ZYNQ7
IMX IP Core configured for 4 channels, 12bit pixels			
Registers	1544	1544	1544
Lookup Tables	1722	1722	1722
BlockRAMs	1	1	1
IMX IP Core configured for 8 channels, 12bit pixels			
Registers	2064	2064	2064
Lookup Tables	2352	2352	2352
BlockRAMs	1	1	1
IMX IP Core configured for 16 channels, 12bit pixels			
Registers	3104	3104	3104
Lookup Tables	3599	3599	3599
BlockRAMs	1	1	1

LEGEND

Included	•
Optional	o
Please contact us	-

AVAILABLE SENSOR

MODULE	SENSOR BOARD AVAILABLE	VERIFIED IN THIRD PARTY HARDWARE	VERIFIED IN SIMULATION
IMX174	✓	✓	✓
IMX249		✓	✓
IMX302			✓
IMX252	✓	✓	✓
IMX265		✓	✓
IMX250	✓	✓	✓
IMX264		✓	✓
IMX255	✓	✓	✓
IMX267		✓	✓
IMX305			✓
IMX253	✓	✓	✓
IMX304			✓
IMX273	✓	✓	✓
IMX296		✓	✓
IMX287			✓
IMX297			✓